REMARKS

Applicants have received the Office Action mailed on 04/24/2006 from Christie, Parker and Hale, LLP.

Applicants submit that this Office Action has been mailed to Christie, Parker, and Hale, LLP by mistake. Applicants respectfully request the Examiner to send future correspondence to the address provided herewith.

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-30 are pending. Claims 1-30 stand rejected.

Claims 1, 3, 4, 15, 23, 25, and 30 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicant submits that the amendments do not add new matter.

Applicant reserves the rights with respect to the applicability of the Doctrine of Equivalents.

DOUBLE PATENTING REJECTION

Claims 1-12, 14-26, and 28-30 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-12, 14-26, and 28-30, respectively, of co-pending Application No. 09/951750.

Applicants herein defer response to the double patenting rejection because it is provisional. Applicants will attend to the double patenting rejection at a later time, if a co-pending Application No. 09/951750 matures into a patent.

REJECTIONS UNDER 35 U.S.C. § 112

The Examiner has rejected claim 13 under 35 U.S.C. §112, second paragraph, as failing to set forth the subject matter which applicant regards as their invention. The Examiner stated that

> "The capacitance is distributed gate capacitance".... indicates that the invention is different from what is defined in the claim, because the invention is about interconnection. The capacitance in this claim is capacitance of interconnection between devices, a driver, and a receiver, while gate capacitance is a capacitance of a transistor device, which is a portion of the receiver; technically and conventionally it cannot be considered a part of interconnection.

(Office Action, p. 4, 04/24/06)

Applicants respectfully disagree. The instant Specification discloses the following:

> It is possible to obtain more precise approximations of the interconnection within the scope of the present invention by using more complex test RC networks. Alternative embodiments may employ multiple RC networks using poly resistance and distributed gate capacitance. A more precise model may be created by including additional parameters (e.g., the dielectric loss of the PCB traces). The same can be made adaptive by having programmable resistive and capacitive components so different topologies of the IO link could be emulated.

(Specification, paragraph [0021], p. 7).

Thus, the instant Specification discloses that it is possible to obtain more precise approximations of the interconnection within the scope of the present invention by using more complex test RC networks. Alternative embodiments may employ multiple RC networks using poly resistance and distributed gate capacitance.

Therefore, Applicants respectfully submit that claim 13 does set forth the invention in clear and concise language. In view of this, Applicant requests the Examiner to withdraw th rejection under 35 U.S.C. §112, second paragraph.

REJECTIONS UNDER 35 U.S.C. § 102

Claims 1-30 have been rejected under 35 U.S.C. § 102(b) as being unpatented by Neil Weste, et al., "Principles of CMOS VLSI Design: A System Perspective, Second Edition, 1993, Addison-Wesley Publishing Company" (hereinafter "Weste").

Applicants have amended claim 1 to include measuring first electrical characteristics of an interconnection, including generating a first graphical representation of an output of interconnection that is based, at least in part, on the first electrical characteristics; and determining a test network having second electrical characteristics such that the first electrical characteristics of the interconnection are approximated by the second electrical characteristics of the test network within a specified tolerance, wherein determining the test network includes adjusting the second characteristics based on the first graphical representation.

Weste discloses characterization and performance estimation of a circuit. More specifically, Weste discloses determining of the resistance and capacitance of the circuit components using formulas (pp. 176-179, pp. 191-198) and modeling (p. 191, paragraph 3, p. 198, paragraphs 2-4). Further, Weste discloses that a long wire can be represented in terms of several RC sections (formulas 4.24 - 4.28, pgs. 199-200, Fig. 4.15). In particular, Weste discloses the current-voltage characteristics of operation of a CMOS inverter according to the analytical delay model (p. 207-209, Figure 4.18).

Thus, Weste merely discloses the graphical representation of the analytical model of operation of a component. In contrast, amended claim 1 refers to measuring first electrical characteristics of an interconnection, including generating a first graphical representation of an output of interconnection that is based, at least in part, on the first electrical characteristics.

Further, Weste merely discloses that a long wire can be represented by RC sections, in contrast to determining a test network having second electrical characteristics such that the first

electrical characteristics of the interconnection are approximated by the second electrical characteristics of the test network within a specified tolerance, wherein the determining includes adjusting the second characteristics based on the first graphical representation, as recited in amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not anticipated by Weste under 35 U.S.C. § 102(b).

Because claims 2-14, 15-22, and 23-30 contain related limitations, Applicants respectfully submit that claims 2-14, 15-22, and 23-30 are not anticipated by Weste under 35 U.S.C. § 102(b).

CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: August 24, 2006 By: _____

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